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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/010,273	12/05/2001	Hiroaki Asada	10873.851US01	5636

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EXAMINER	
NGUYEN, VAN THU T	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 06/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/010,273	ASADA, HIROAKI
	Examiner	Art Unit
	VanThu Nguyen	2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 6-13 is/are allowed.

6)☒ Claim(s) 1-5 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 12/05/2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 03/14/2002.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-13 are present for examination.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: MEMORY DEVICE HAVING ADDRESS GENERATING CIRCUIT USING PHASE ADJUSTMENT BY SAMPLING DIVIDED CLOCK TO GENERATE ADDRESS SIGNAL OF SEVERAL BITS HAVING ONE BIT CHANGED IN SEQUENTIAL ORDER

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3, 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Futatsuya et al. (U.S. Patent No. 5,602,778).

Regarding claim 1, Futatsuya discloses a semiconductor integrated circuit device (see FIG. 1) incorporating a semiconductor memory circuit (Memory Cell Array 100, see FIG. 1) and a control circuit (see 110 of FIG. 1, or Address Control Circuit in FIG. 32) for controlling a data access to the semiconductor memory circuit, wherein the control circuit outputs an address signal of several bits (G0-G9 to Address Determining Circuit, see FIG. 32) in which only a value of 1 bit changes in a sequential order (see example of Gray Code g0-g3 in FIG. 31) when a data

access by consecutive addresses is performed on the semiconductor memory circuit (see corresponding binary code a0-a3 in FIG. 31).

Regarding claim 3, it is rejected under U.S.C. 102(b) because it recites similar limitations as in claim 1.

Regarding claim 5, Futatsuya also discloses means for converting a location of data stored in the semiconductor memory circuit into a location corresponding to a change in the address signal from the address generation circuit (120 and 116, see FIG. 1).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2, 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Futatsuya et al. in view of APA (Admitted Prior Art FIG. 10).

Futatsuya discloses, as applied in prior rejection of claim 1, all claimed subject matter except the Memory Cell Array 100 is a non-volatile memory.

APA disclose, on page 1, the semiconductor memory circuit is a ROM.

Since Futatsuya and APA are both from the same field of endeavor, the purpose disclosed by APA would have been recognized in the pertinent art of Futatsuya et al..

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to replace the non-volatile memory array in Futatsuya with a ROM in APA because all memory types require address to access.

Regarding claim 4, it is rejected under U.S.C. 103(a) because it recites similar limitations as in claim 2.

Allowable Subject Matter

7. Claims 6-13 are allowed.

The following is a statement of reasons for the indication of allowance:

The prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Futatsuya, Clark et (U.S. Patent 6,509,851), Sugibayashi (U.S. Patent 5,986,942) and Sato et al. (U.S. Patent 5,497,353) taken individually or in combination, do not teach the claimed invention having the following limitations, in combination with the remaining claimed limitations:

i) wherein the control circuit includes an address generation circuit that divides a clock to be input, performs a phase adjustment by sampling the divided clock and generates an address signal of several bits (as in claim 6); or

ii) wherein the control circuit includes an address generation circuit that divides a clock to be input and generates an address signal of several (m) bits in which bit 0 is set as a lowest-order bit, and the address generation circuit outputs the address signal of several bits in which only a value of 1 bit changes in a sequential order by dividing the clock by (1/4).times.$(1/2)^i$ to generate bit i (i=0 to (m-1)) and delaying a phase of each bit by 1/4 cycle with respect to a cycle of an immediately lower-order bit when a data access by consecutive addresses is performed on the semiconductor memory circuit (as in claim 12); or

ii) a counter register that stores a divided clock corresponding to an immediately

higher-order bit as data based on a divided clock corresponding to a low-order bit to be output from the counter circuit and outputs a count value (as in claim 12).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Sato and Sugibayashi in teaching of claims 1-5.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Friday, 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 17, 2005

VanThu Nguyen
Primary Examiner
Art Unit 2824